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PATENT
8031-1028

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Yoshihiro NONAKA

Conf. 5218

Application No. 10/648,256

Group 2811

Filed August 27, 2003

Examiner O. Nadav

SEMICONDUCTOR INTEGRATED CIRCUIT,
METHOD OF MANUFACTURING SEMICONDUCTOR
INTEGRATED CIRCUIT, CHARGE PUMP CIRCUIT,
LAYOUT DESIGNING APPARATUS, AND LAYOUT
DESIGNING PROGRAM

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying document, a copy of which is attached to this statement, is made of record on the enclosed Form PTO-1449.

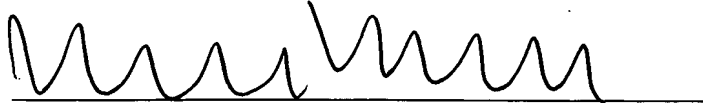
A concise explanation of the relevance of this item is that this reference was cited by the Chinese Patent Office in the corresponding Chinese Application Serial No. 03158127.7. A copy of the Chinese Official Action and English translation in which it was cited is attached hereto.

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign Patent Office in a

counterpart foreign application not more than three months
prior to the filing of this Statement.

Respectfully submitted,

YOUNG & THOMPSON

A handwritten signature in black ink, appearing to read 'Robert J. Patch', written over a horizontal line.

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RJP/lk

September 1, 2005

Application No.:
10/648,256

Applicant:
Yoshihiro NONAKA

Filing Date:
August 27, 2003

Group Art Unit:
2811

[illegible][illegible]

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

* Abstract provided for the Examiner's convenience